APPENDIX A
"CLEAN" VERSION OF EACH PARAGRAPH/SECTION/CLAIM
37 C.F.R. § 1.121(b)(ii) AND (c)(i)

SPECIFICATION:

Paragraph at page 2, line 16 to line 20:

Because of these diverse requirements, different manufacturing processes are used for a "megarad" product, designed for use in a high total radiation dose environment, and an SEE product which is optimized for single particle effects.

Paragraph at page 3, line 1 to line 17:

BRIEF DESCRIPTION OF THE INVENTION

In accordance with the present invention a MOSgated device (a power MOSFET, IGBT, GTO or other device employing a MOS gate) which has optimal oxide thicknesses for both total radiation dose resistance and SEE resistance is provided, using a trench design device. Thus, a known vertical conduction trench device has an invertible channel region on the sides of each trench, while the drift region lies along and under the bottoms of the trenches. Consequently, the gate oxide thickness at the walls of each trench can be relatively thin, and less than about 900 Å (preferably about 500 Å) for optimal total dose resistance, while the bottoms of the trenches have a relatively thick oxide liner, for example, greater than about 1300 Å (and preferably about 3000 Å) for optimal resistance to breakdown by single event effects.

Paragraph at page 5, line 6 to line 17:

Thereafter, the wells 20 to 23 are filled with conductive N+ polysilicon layers 50 to 53 which act as the conductive gates for the device and which are laterally interconnected (not shown) and have an appropriate common gate connection terminal G. The tops of polysilicon layers 50 to 53 are covered by patterned oxide insulation layers 60 to 63 respectively. The upper

surface of the device then receives an aluminum source electrode 70 which is connected to the exposed regions of source regions 14 to 17, and to the P regions 13 between the sources. A drain electrode 71 is formed on the bottom of chip 10.

Insert Paragraph at page 6 between lines 8 and 9:

Trenches containing MOS gated structure 20, 21 may be polygonal in topology and may be symmetrically spaced and disposed over the surface of the chip 10. Source regions 14, 15 surround trenches 20, 21, respectively, containing MOS gated structure. Intermediate trenches 80-82 may consist of a trench of lattice shape in topology extending in the space defined between spaced polygonal trenches 20, 21.

Paragraph at page 9, line 25 to page 10, line 3:

The trenches may provide a plurality of floating rings, or at least one floating ring. The precise number of trenches used and their spacing can be optimized for each voltage rating. Thus, more rings with wider spacing are used for higher voltage devices and fewer rings at closer spacing are used for lower voltage ratings. For example, for a high voltage termination, the rings may be spaced by 3 to 5 microns. For a lower voltage termination, the rings could be spaced from 1.5 to about 2 microns. The wider spaced rings will break down at a lower voltage than closer spaced rings.

CLAIMS (with indication of amended or new):

(NEW) 29. A trench MOS gated device which has improved resistance to both high radiation and single event high energy charged particles (SEE), comprising:

a silicon wafer of one conductivity type having a plurality of spaced shallow active trenches containing respective gate structures and a plurality of intermediate trenches each disposed between a respective pair of active trenches;

each of said active trenches and each of said intermediate trenches having at least partly vertical walls joined at their bottoms by respective trench bottoms;